



**OL\_H264E-CFS**  
**HDTV H.264/AVC Video**  
**Encoder**  
**With Compressed Frame Store**  
Rev 1.0

## General Description

The OL\_H264E-CFS core is a hardware implementation of the H.264 video compression algorithm. The core accepts up to the highest resolution HDTV video stream as input and outputs the encoded bitstream.

Simple, fully synchronous design with low gate count.

## Applications

- ◆ Digital video recorders.
- ◆ Video wireless devices.
- ◆ Video surveillance systems.
- ◆ Hand held HDTV video cameras.

## Features

- ◆ Fully compatible with the ITU-T H.264 specification.
- ◆ Highly (10-15:1 ) compressed frame store (CFS) with perfect reconstruction (no error/drift) with third party standard decoders. Patent pending technology.
- ◆ Extremely low power : no external DRAM required and much lower bandwidth and power through the CFS.
- ◆ I and P frame support.
- ◆ Proven in FPGA : 720p @ 30 fps in Virtex5-2 demo board with video streamed to Ethernet.
- ◆ Profile level 4.1, can be decoded by Baseline, Main or Hi Profile decoder.
- ◆ Supports up to the highest HDTV video resolution (1920x1080 @ 30 fps progressive).
- ◆ Very low operational frequency : from ~1.5 MHz for QCIF @ 15 fps to ~250 MHz for 1920x1080 @ 30 fps.
- ◆ Single core HDTV support in FPGA : 720p (1280x720) at 30 fps in high end device.
- ◆ No CPU required for encoding.
- ◆ Constant Bit Rate (CBR). Partial Variable Bit Rate (VBR).
- ◆ Very low latency (~1.1 ms for VGA @ 30 fps).
- ◆ Motion vector up to -16.00/+15.75 pixels around the predicted motion vector (-24.00/+23.75 around the origin), down to quarter pixel.
- ◆ Support for most of intra4x4 and all intra16x16 modes.
- ◆ Block skipping logic for lower bitrate.
- ◆ Supports YUV 4:2:0 video input.
- ◆ Min Clock speed = ~ 4 x the raw pixel clock speed.
- ◆ Low gate count : 280 K gates + 217 Kbits of RAM for real time 1080p @ 30
- ◆ Simple, fully synchronous design.
- ◆ Available as fully functional and synthesizable VHDL or Verilog soft-core.

## **OL\_H264E-CFS : HDTV H.264/AVC Video Encoder with CFS**

### **Functional Description**

The OL\_H264E-CFS core is a hardware implementation of the H.264 video compression algorithm designed to process HDTV progressive video up to 1920x1080 at 30 fps.

Each block of 16x16 pixels is processed in just 1024 cycles. This means that each pixel is processed in just 4 cycles. Consequently, given an uncompressed video stream of resolution X by Y, and frame rate fps, the minimum clock frequency to process a such video stream is :

$$F = 4 * X * Y * fps$$

This allows the core to process the video stream at relatively low clock frequencies. For example, HDTV video of 1920x1080 @ 30 fps requires ~250 MHz, whereas VGA video of 640x480 @ 30 fps requires ~37 MHz.

The table below summarizes the relationship between some possible video resolutions and frame rates and the clock frequency of the core.

Resolution	QCIF @ 15 fps	CIF @ 30fps	VGA @ 30fps	1280x720 @ 30fps	1920x1080 @ 30fps
Core freq.	~1.5 MHz	~12.1 MHz	~36.8 MHz	~110.5 MHz	~250.6 MHz

**Table 1 Core frequency versus video resolution and frame rate.**

### **Advantages of the core**

Some of the key advantages of the core are discussed further below:

#### **Compressed Frame Store (CFS)**

The core stores reference images used during motion estimation in a compressed frame store (CFS) using patent pending technology. Depending on the quality required in the H.264 encoded bitstream, compression in the CFS can be as high as 10-15:1. No reconstruction error or drift is present when the output H.264 bitstream is decoded with a third party, standard, decoder.

The table below details the approximate uncompressed reference frame storage requirement for various video resolutions, compared to that required for CFS with an average of ~250 bits/macroblock. This is a 24:1 reduction in external memory compared to the OL\_H264E core that requires two full frames of 4:2:0 video.

Resolution	VGA 640x480	D1 720x480	720p 1280x720	1080p 1920x1080
Uncompressed size	450	506.25	1350	3060
Compressed size	~38.4	~43.2	~115.5	~261.2

**Table 2 Frame store size comparison, figures in Kbytes (1024 bytes)**

The above is only an example and a smaller CFS is possible with lower and still perfectly acceptable quality.

Such low amounts of memory required, even for HDTV, allows direct integration of the CFS memory in a SoC as a single port SRAM, without the need for expensive and power hungry DRAM.

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### **Extreme Low Power**

The CFS brings the additional advantage of extreme low power:

- No expensive and power hungry DRAM required
- No power hungry, fast interface to the external DRAM on the printed circuit board
- Because the data in the CFS is highly compressed, the access to the external memory is sporadic. This means much lower bandwidth and, hence, power.

### **HDTV support**

The core is designed to support up to the highest HDTV resolution, 1920x1080 @ 30 fps progressive. This opens a whole new range of applications from consumer video camcorders to high-resolution video surveillance at very low cost.

### **Low gate count**

As it can be seen in the **Performance** section below, the core is designed very efficiently, with a low gate count. This allows 4CIF (704x576) video @ 30 fps to be processed by low end FPGAs as well as 720p (1280x720) video @ 30 fps in high end FPGAs.

The low gate count also results in low power.

### **Progressive and interlaced video support**

The core can support both progressive and interlaced video, for maximum flexibility. When encoding progressive video, the output can be compatible with Baseline, Main and Hi profile decoders. When encoding interlaced video, the output is compatible Main and Hi profile decoders.

### **Extremely low latency**

Encoding latency is only 16 lines of video. This means that the encoder starts outputting a valid bitstream almost immediately after video is fed in. This feature is vital for a variety of applications such as videoconferencing and mobile videophones. The table below lists the encoding latency for some resolutions and frame rates.

Resolution	QCIF @ 15 fps	CIF @ 30fps	VGA @ 30fps	1280x720 @ 30fps	1920x1080 @ 30fps
Latency	~7.4 ms	~1.85 ms	~1.1 ms	~0.75 ms	~0.5 ms

**Table 2 Core encoding latency versus video resolution and frame rate.**

### **No external CPU required**

The core can encode video independently, without the support of an additional CPU. This represents a large cost saving compared to solutions that require an external CPU.

### **CBR and partial VBR supported**

The core supports CBR (Constant Bit Rate). VBR (Variable Bit Rate) can only be partially supported in order to prevent the CFS from overflowing.

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### **Performance**

Performance figures of the OL\_H264E-CFS core implemented with some particular technologies are shown in the table below. All the features listed above are included in the gate count.

Technology	Approx Area	Speed	Video Throughput
0.13 $\mu$ LV 0.9V, 125 C	280 Kgates + 217 Kbits RAM + CFS memory	$\sim$ 250 MHz	1920x1080 (1080p) @ 30 fps
	FPGA data to be released soon		

**Table 3 Performance of the OL\_H264E-CFS core**

### **Summary**

The combination of low gate count, low operating frequency, low power, and full HDTV resolution support makes this core an application-enabling technology.

The presence of the CFS with such high compression instead of a standard external reference frame store makes this core unique for its low resource and power requirements.

This core is suitable for a wide range of applications including mobile phones, camcorders, webcams and video surveillance cameras.

The very small footprint of this core also facilitates novel applications such as its direct integration on to a CMOS sensor. This would create an extremely compact intelligent sensor accepting light directly at its input and outputting an H.264 bitstream.

### **Deliverables**

Synthesizable VHDL or Verilog RTL.  
Bit accurate C model.  
Complete HDL testbench.  
Complete data sheet.

### **Ocean Logic Pty Ltd**

PO BOX 768 - Manly NSW 1655 - Australia Fax: +61-2-90120979  
E-Mail: [contact@ocean-logic.com](mailto:contact@ocean-logic.com) URL : <http://www.ocean-logic.com/>