

OL_H264MCLD
Multi-Channel HDTV
H.264/AVC Limited
Baseline Video
Decoder
V1.0

General Description

The OL_H264MCLD core is a hardware implementation of the H.264 baseline video compression algorithm. The core decodes a bitstream produced by the OLH264e encoder and produces a video stream up to the highest HDTV resolution. Simple, fully synchronous design with low gate count.

Applications

- ◆ Digital video recorders.
- ◆ Video wireless devices.
- ◆ Video surveillance systems.
- ◆ Hand held HDTV video cameras.

Features

- ◆ Fully compatible with the output of the OL_H264MCE encoder core.
- ◆ Up to Profile level 4.1 can be decoded.
- ◆ Supports up to the highest HDTV video resolution (1920x1080 @ 30 fps progressive).
- ◆ Very low operational frequency : from ~1.5 MHz for QCIF @ 15 fps to ~250 MHz for 1920x1080 @ 30 fps.
- ◆ Direct support for both progressive and interlaced video.
- ◆ Single core HDTV support in FPGA : 720p (1280x720) at 30 fps in high end FPGAs (Virtex4) . 4 CIF (704x576) at 30 fps in low end FPGAs.
- ◆ No CPU required for decoding.
- ◆ Very low latency decoding
- ◆ Motion vector up to -32.00/+31.75 pixels.
- ◆ Support for most of intra4x4 and all intra16x16 modes.
- ◆ Multiple slices support for better error resilience.
- ◆ Block skipping logic for lower bitrate.
- ◆ Deblocking filter for better quality.
- ◆ External memory interface tolerant of high latencies and delays, ideal in a SoC system or in a shared bus with a CPU. The memory interface can be clocked at a different frequency from the core for easier integration.
- ◆ Supports YUV 4:2:0 video output.
- ◆ Min Clock speed = 4 x the raw pixel clock speed.
- ◆ Simple, fully synchronous design.
- ◆ Available as fully functional and synthesizable VHDL or Verilog soft-core.

OL_H264MCLD : HDTV H.264/AVC Limited Baseline Video Decoder

Functional Description

The OL_H264MCLD core is a hardware implementation of the H.264 baseline video compression algorithm designed to decode a bitstream created by the OL_H264e core and output progressive video up to HDTV 1920x1080 at 30 fps.

Each block of 16x16 pixels is processed in just 1024 cycles. This means that each pixel is processed in just 4 cycles. Consequently, given an target video stream of resolution X by Y, and frame rate fps, the minimum clock frequency to decode a such bitstream is:

$$F = 4 * X * Y * fps$$

This allows the core to process the video stream at relatively low clock frequencies. For example, HDTV video of 1920x1080 @ 30 fps requires ~250 MHz, whereas VGA video of 640x480 @ 30 fps requires ~37 MHz.

The table below summarizes the relationship between some possible video resolutions and frame rates and the clock frequency of the core.

Resolution	QCIF @ 15 fps	CIF @ 30fps	VGA @ 30fps	1280x720 @ 30fps	1920x1080 @ 30fps
Core freq.	~1.5 MHz	~12.1 MHz	~36.8 MHz	~110.5 MHz	~250.6 MHz

Table 1 Core frequency versus video resolution and frame rate.

A block diagram of the core is shown in Figure 1.

The NAL decoding unit parses the incoming bitstream extracting the block residual information as well as other syntax elements.

The block residual information is inverse quantized and transformed before being added to the prediction data.

Such prediction data is generated by either the intra or inter prediction unit, according to the decoded syntax elements.

The intra prediction unit is capable of generating a prediction for all intra16x16 modes as well as the supported intra4x4 modes.

The inter prediction unit can generate a prediction using a single motion vector down to ¼ pixel. The subpixels are generated according to the interpolation filters specified in the ITU-T H.264 baseline specification.

Each macroblock is optionally filtered, according to the information extracted from the bitstream, before being output.

A reconstructed macroblock is also stored in the external memory in order to be subsequently used by the inter prediction unit.

OL_H264MCLD : HDTV H.264/AVC Limited Baseline Video Decoder

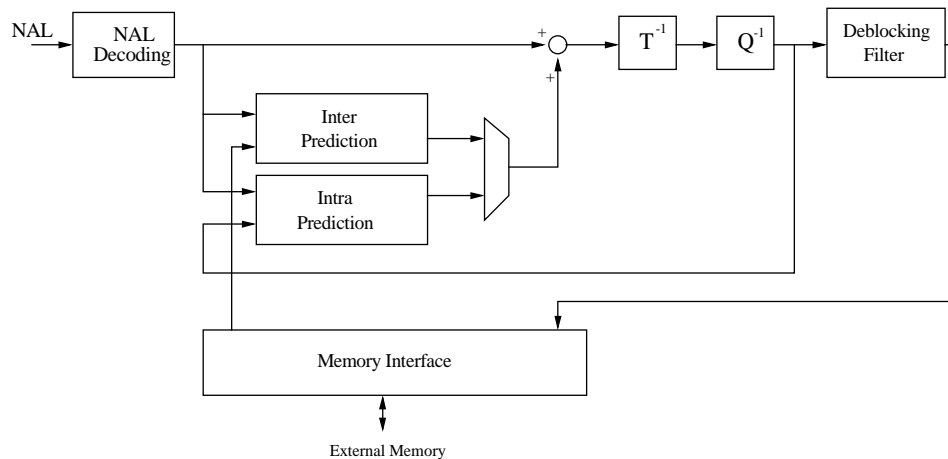


Figure 1 The OL_H264MCLD block diagram.

Advantages of the core

Some of the key advantages of the core are discussed further below:

HDTV support

The core is designed to support up to the highest HDTV resolution, 1920x1080 @ 30 fps progressive. This opens a whole new range of applications from high-end video camcorders to high-resolution video surveillance at very low cost.

Low gate count

The core is designed very efficiently, with a low gate count. This allows 4CIF (704x576) video @ 30 fps to be decoded by low end FPGAs at the slowest speed grade as well as 720p (1280x720) video @ 30 fps in high end FPGAs.

Multi-channel support

The pixel processing capability of the core can be shared among multiple video channels (up to 32). Each video channel can have its own resolution and switching from one channel to the other will happen on the frame boundary. For example, at 250 MHz, up to 6 D1 (720x480) channels can be decoded simultaneously at 30 fps or up to 20 CIF (352x288) channels at 30 fps or a combination of both.

This allows for a very flexible decoding environment where multiple channels with different resolutions and frame rates are decoded by the same small core.

Progressive and interlaced video support

The core can support both progressive and interlaced video, for maximum flexibility.

No external CPU required

The core can decode video independently, without the support of an additional CPU. This represents a large cost saving compared to solutions that require an external CPU.

OL_H264MCLD : HDTV H.264/AVC Limited Baseline Video Decoder

Flexible memory interface

The core requires access to an external memory via a 32-bit data bus. About 50% of the whole theoretical bandwidth of the memory is actually used by the core.

This interface is designed to be independent from the memory used (i.e. DDR, SDRAM, SRAM, etc.).

More importantly, the memory interface is designed to tolerate high and unpredictable latencies and delays that are typical of a shared memory (i.e. AMBA and/or SoC where the bus is shared with a CPU or other cores).

In addition to this the memory interface can run at a different clock speed from the rest of the core. This simplifies the integration process and can save gates by not forcing the core to be synthesised to a much higher frequency just to be synchronous with the local bus.

This allows, for example, a core running at 37 MHz (decoding VGA @ 30 fps) to be easily integrated in a SoC sharing a 200 MHz bus with a processor.

Error resilience

The core supports multiple slices. This is useful in environments prone to data transmission problems (i.e. mobile phone or other wireless applications) in order to limit the damage inflicted to the image by transmission errors.

Low data rate features

The core supports two important features for low data rates: deblocking filter and macroblock skipping.

The deblocking filter especially improves the visual quality of the decoded image at low bitrates where the high quantisation noise produces unappealing "blockiness" in an image.

Macroblock skipping greatly reduces the bitrate with minimal effect on the visual quality of the decoded image.

Performances

Performance figures of the OL_H264MCLD core implemented with some particular technologies are shown in the table below. All the features listed above are included in the gate count.

Technology	Approx Area	Speed	Video Throughput
0.13 u LV 0.9V, 125 C	70 Kgates + 79 Kbits RAM Optimised for speed	~ 250 MHz	1920x1080 (1080p) @ 30 fps
StratixII	6949 ALUTs + 1 M512 + 45 M4K + 1 DSPs	~113 MHz	1280x720 (720p) @ > 30 fps
Virtex4-12	4100 slices + 1 multipliers + 21 RAM blocks	~110 MHz	1280x720 (720p) @ 30 fps

Table 2 Performance of the OL_H264MCLD core.

Summary

The combination of low gate count, low operating frequency, and full HDTV resolution support makes this core an application-enabling technology.

The applications of this core range from low power wireless application at relatively low resolution such as mobile phones to HDTV handheld recorders and video surveillance cameras.

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Deliverables

Synthesizable VHDL or Verilog RTL.
Bit accurate C model.
Complete HDL testbench.
Complete data sheet.

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